

FIG. 1 (Related Art)

Translation of Macro Instructions into Native Instructions

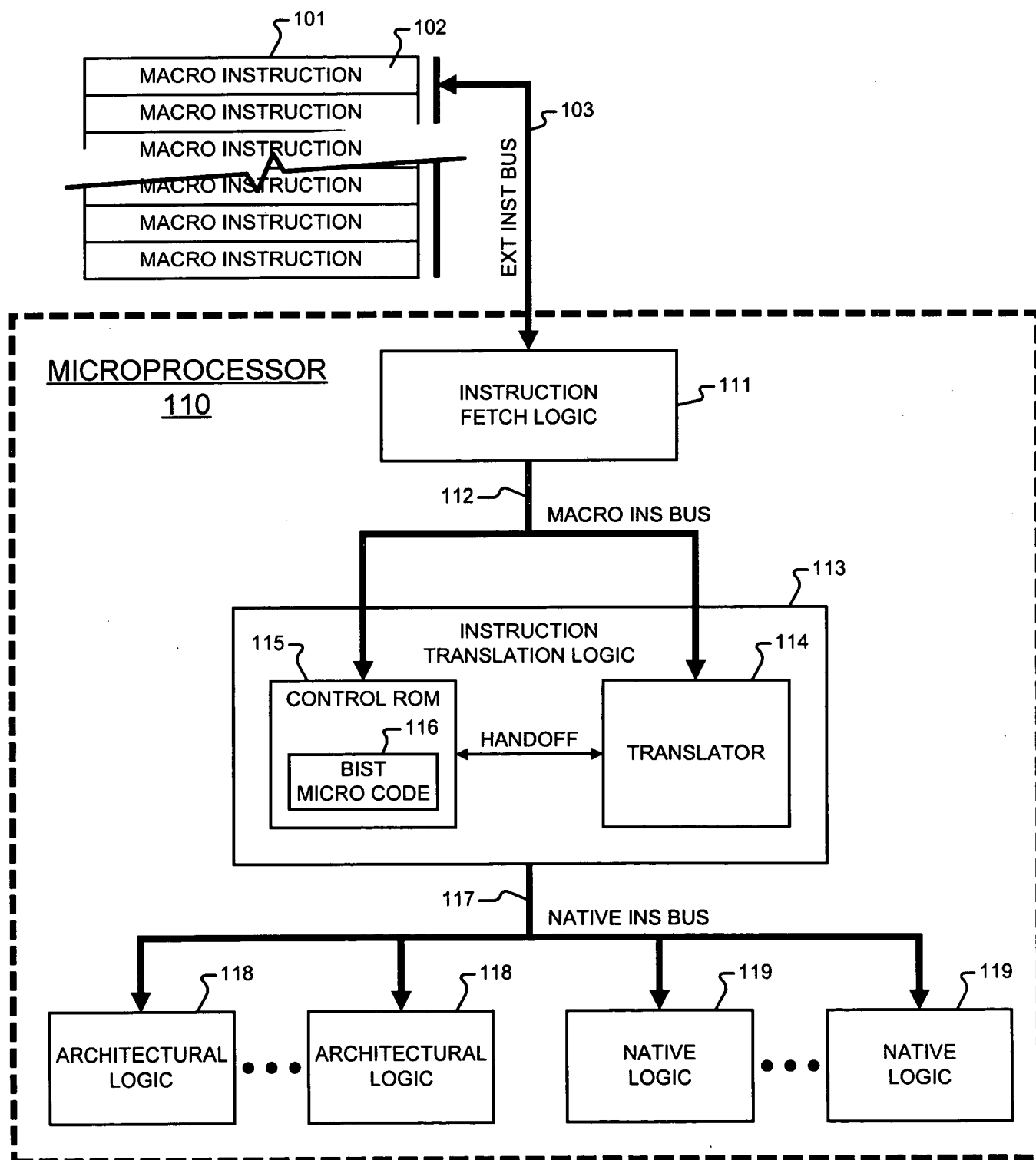


FIG. 2 (Related Art)

Indirect Specification of Native Register via Macro Instruction

200

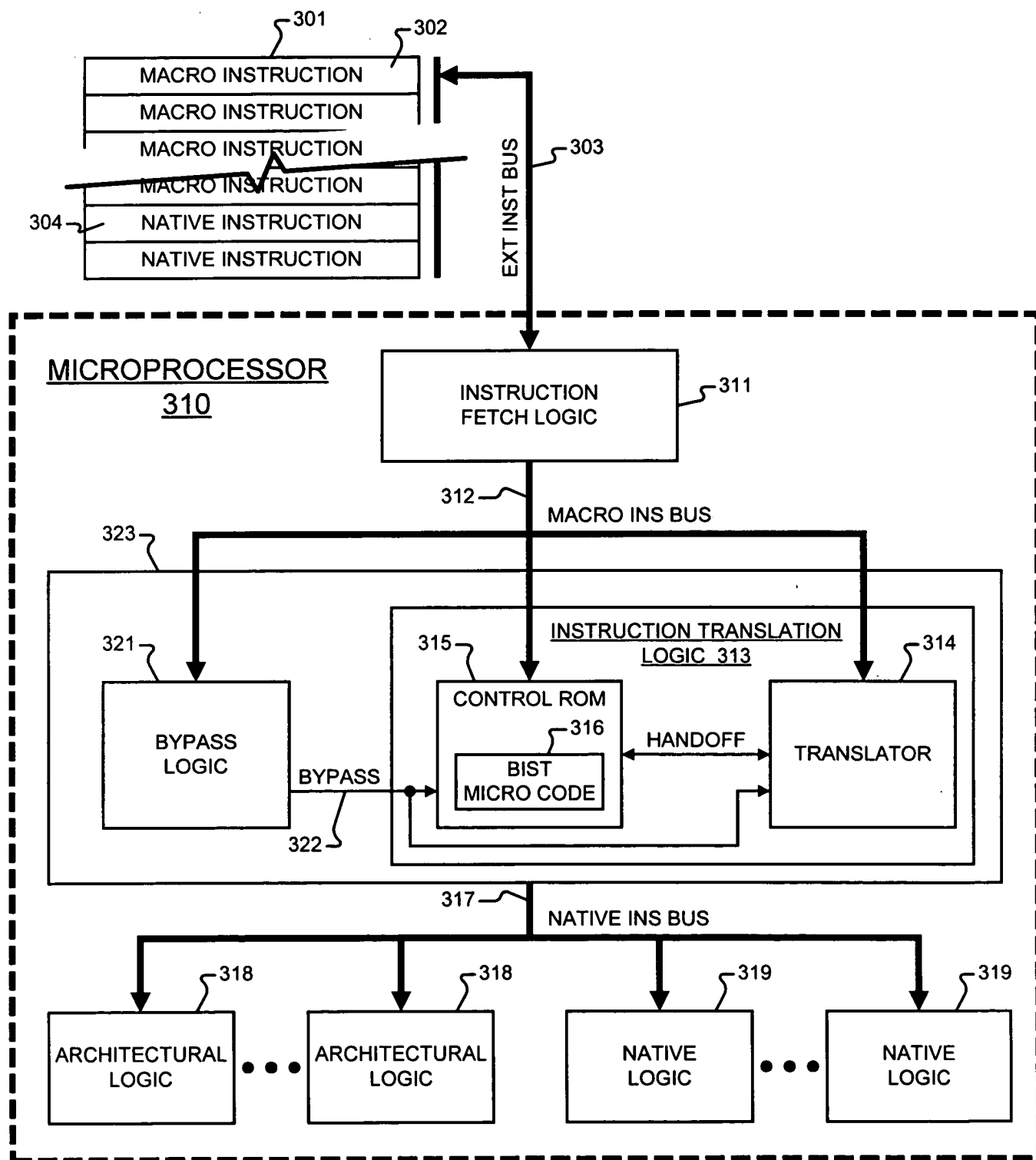
| Cycle | Macro Ins Bus       | Native Ins Bus        |
|-------|---------------------|-----------------------|
| 1     | ADD [EAX],FFFFFFFFh | ***                   |
| 2     | ***                 | LD NR1,[EAX]          |
| 3     | ***                 | ADD NR1,NR1,FFFFFFFFh |
| 4     | ***                 | ST [EAX],NR1          |

3 CYCLES

FIG. 3

Translator Bypass for Native Instructions

300



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FIG. 4

Translate Stage Logic for Native Instruction Bypass Mode

400

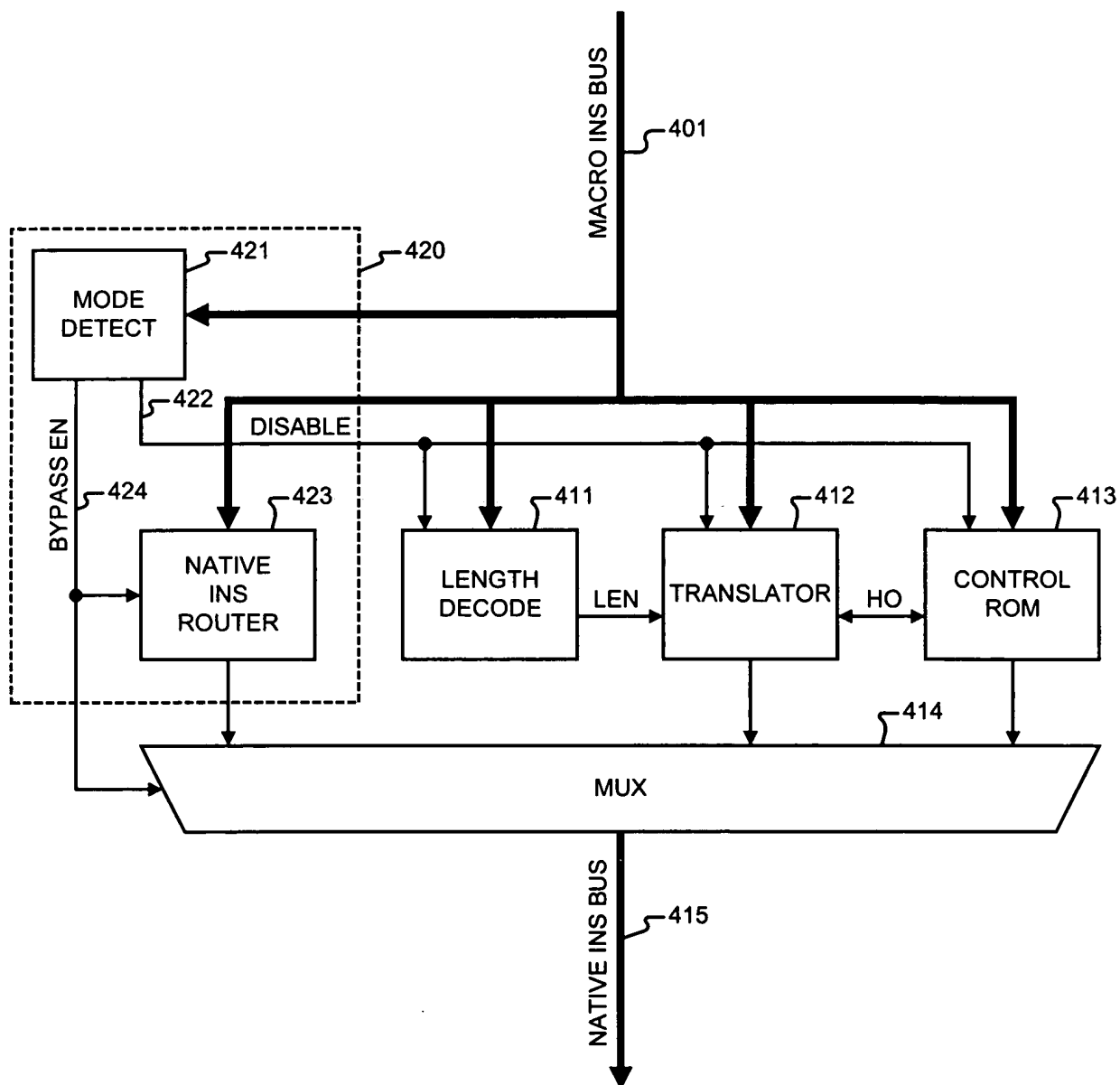


FIG. 5

Using Microcode to Test Native Resources

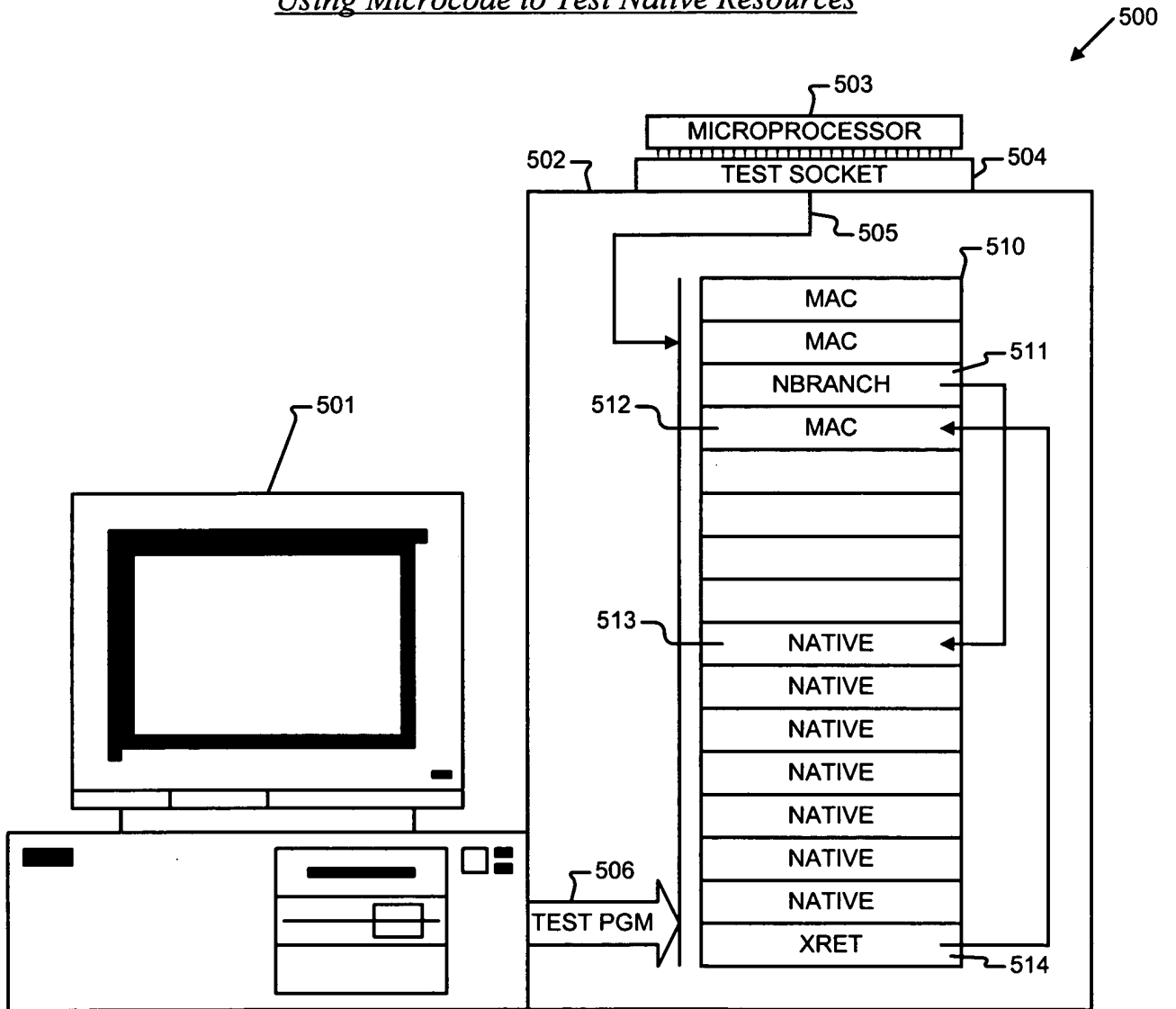


FIG. 6

Instruction Sequence for Testing Native Registers

600

| Cycle | Macro Ins Bus  | Native Ins Bus |
|-------|----------------|----------------|
| 1     | MOV EAX,TST1   | +++            |
| 2     | MOV EBX,OUTBFR | LD EAX,TST1    |
| 3     | NBRANCH        | LD EBX,OUTBFR  |
| 4     | LD T1,0        | JMP [EAX]      |
| 5     | ST [EBX],T1    | LD T1,0        |
| 6     | NOT T1         | ST [EBX],T1    |
| 7     | ST [EBX],T1    | NOT T1         |
| 8     | +++            | ST [EBX],T1    |
| 9     | +++            | +++            |
| 10    | +++            | +++            |
| 1001  | XRET           | +++            |
| 1002  | NEXT MAC       | JMP [EAX+1]    |
| 1003  | +++            | NEXT MAC       |

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